CLAIMS

What is claimed is:

1. A method comprising:

translating instructions from a source instruction set architecture (ISA) having a segmented memory addressing model into a target ISA having a non-segmented memory addressing model;

executing the translated instructions; and

simulating, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions.

2. The method of claim 1, wherein translating instructions comprises:

detecting a segment table update; and

updating a segment table maintained by the target ISA according to the detected segment table update.

3. The method of claim 2, wherein detecting the segment table update comprises:

identifying a segment descriptor associated with the segment table update;

determining a segment base address according to the identified segment descriptor; and

storing the segment base address within a target ISA register assigned to a segment described by the identified segment descriptor.

4. The method of claim 2, wherein updating the segment table comprises:

identifying a segment descriptor associated with the segment table update;

inserting the identified segment descriptor within the segment table maintained by the target ISA; and

updating the segment table maintained by the target ISA to identify a target ISA register assigned to a segment described by the identified segment descriptor.

5. The method of claim 1, wherein prior to translating the instructions, the method comprises:

allocating a target ISA segment table to enable a segmented memory addressing model within the target ISA;

designating one or more target ISA registers as segment base registers to contain segment base addresses of segments utilized by a source application; and

allocating a target ISA predicate register for each of the one or more allocated target registers.

6. The method of claim 1, wherein translating comprises:

detecting a segment register update instruction; and

updating a source ISA state according to the segment register update instruction.

7. The method of claim 1, wherein updating the source ISA state comprises:

querying the target ISA segment table according to a segment selector of the detected segment register update instruction;

identifying a target register assigned to a segment described by the segment descriptor within the target segment table; and

setting a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment.

8. The method of claim 1, wherein translating comprises:

identifying each segment descriptor within the target segment table;

assigning a target register to each segment described by an identified segment descriptor;

loading a base address of each segment descriptor within the target register assigned to the segment; and

setting a target ISA predicate register assigned to each identified target register to identify the target register containing a base address of each segment used by a source application thread.

9. The method of claim 1, wherein simulating the segmented addressing model comprises:

identifying a logical address expression in a translated instruction; and

calculating a linear address for the identified logical address according to a target register containing a base address of a segment identified by the logical address.

10. The method of claim 9, wherein calculating the linear address comprises:

determining a segment selector portion of the identified logical address;

identifying a source ISA segment register reference by the segment selector;

querying allocated target predicate registers to identify a target predicate register assigned to the identified source ISA segment register;

detecting a target register containing a base address of the segment identified by the segment selector according to the identified target predicate register; and

adding the base address of the segment to an offset portion of the logical address to compute the linear address within the target ISA memory model.

11. An article of manufacture including a machine readable medium having stored thereon instructions which may be used to program a system to perform a method, comprising:

translating instructions from a source instruction set architecture (ISA) having a segmented memory addressing model into a target ISA having a non-segmented memory addressing model;

executing the translated instructions; and

simulating, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions.

12. The article of manufacture of claim 11, wherein translating instructions comprises:

detecting a segment table update; and

updating a segment table maintained by the target ISA according to the detected segment table update instruction.

13. The article of manufacture of claim 12, wherein detecting the segment table update comprises:

identifying a segment descriptor associated with the segment table update;

determining a segment base address according to the identified segment descriptor; and

storing the segment base address within a target ISA register assigned to a segment described by the identified segment descriptor.

14. The article of manufacture of claim 12, wherein updating the segment table comprises:

identifying a segment descriptor associated with the segment table update;

inserting the identified segment descriptor within the segment table maintained by the target ISA; and

updating the segment table maintained by the target ISA to identify a target ISA register assigned to a segment described by the identified segment descriptor.

15. The article of manufacture of claim 11, wherein translating the instructions the method comprises:

allocating a target ISA segment table to enable a segmented memory addressing model within the target ISA;

designating one or more target ISA registers as segment base registers to contain segment base addresses of segments utilized by a source application; and

allocating a target ISA predicate register for each of the one or more allocated target registers.

16. The article of manufacture of claim 11, wherein translating comprises:

detecting a segment register update instruction; and

updating a source ISA state according to the segment register update instruction.

17. The article of manufacture of claim 11, wherein updating the source ISA state comprises:

querying the target ISA segment table according to a segment selector of the detected segment register update instruction;

identifying a target register assigned to a segment described by the segment descriptor within the target segment table; and

setting a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment.

18. The article of manufacture of claim 11, wherein translating comprises:

identifying each segment descriptor within the target segment table;

assigning a target register to each segment described by an identified segment descriptor

loading a base address of each segment descriptor within the target register assigned to the segment; and

setting a target ISA predicate register assigned to each identified target register to identify the target register containing a base address of each segment used by a source application thread.

19. The article of manufacture of claim 11, wherein simulating the segmented addressing model comprises:

identifying a logical address expression in a translated instruction; and

calculating a linear address for the identified logical address according to a target register containing a base address of a segment identified by the logical address.

20. The article of manufacture of claim 11, wherein calculating the linear address comprises:

determining a segment selector portion of the identified logical address;

identifying a source ISA segment register reference by the segment selector;

querying allocated target predicate registers to identify a target predicate register assigned to the identified source ISA segment register;

detecting a target register containing a base address of the segment identified by the segment selector according to the identified target predicate register; and

adding the base address of the segment to an offset portion of the logical address to compute the linear address within the target ISA memory model.

21. An apparatus, comprising:

a processor; and

a memory coupled to the processor, the memory including a translator to translate instructions from a source instruction set architecture (ISA) having a segmented memory addressing model into a target ISA having a non-segmented memory addressing model, to execute the translated instructions and to simulate, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions.

22. The apparatus of claim 21, wherein the translator is to identify a segment descriptor associated with a detected segment table update, to determine a segment base address according to the identified segment descriptor, and to store the segment base address within a target ISA register assigned to a segment described by the identified segment descriptor.

23. The apparatus of claim 21, wherein the translator is to identify a segment descriptor associated with a detected segment table update, to insert the identified segment descriptor within a segment table maintained by the target ISA, and to update the segment table to identify a target ISA register assigned to a segment described by the identified segment descriptor.

24. The apparatus of claim 21, wherein the translator is to query a segment table maintained by the target ISA according to a segment selector of a detected segment register update, to identify a target register assigned to a segment described by the segment descriptor within the segment table, and to set a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment.

25. The apparatus of claim 21, wherein the translator is to identify each segment descriptor within a segment table maintained by the target ISA, to assign a target register to each segment described by an identified segment descriptor, to load a base address of each segment descriptor within the target register assigned to the segment, and

to set a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment.

26. A system comprising:

a chipset;

a double data rate (DDR) synchronous dynamic random access memory (SDRAM) (DDR-SDRAM) memory coupled to the chipset, the memory including a translator to translate instructions from a source instruction set architecture (ISA) having a segmented memory addressing model into a target ISA having a non-segmented memory addressing model, to execute the translated instructions and to simulate, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions.

27. The system of claim 26, wherein the chipset further comprises:

a memory controller coupled to the memory,

28. The system of claim 27, wherein the chipset further comprises:

an input/output (I/O) controller coupled to the memory controller.

29. The system of claim 27, wherein the chipset further comprises:

a graphics controller coupled to the memory controller.

30. The system of claim 27, further comprising:

a processor coupled to the chipset via a front side bus.